```
RCS file: /s6/cvsroot/euterpe/BOM,v
Working file: BOM
head: 5.105
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1940;  selected revisions: 9
description:
top level BOM
----------------------------
revision 3.898
date: 1995/07/07 01:47:42;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at
      Makefile

at/Makefile:  Didn't have $(PERL) selecting the interpreter for
   at/genatpasel.pl, allowing it to select its own and depend on it
   being of executable file mode.
----------------------------
revision 3.897
date: 1995/07/06 06:05:30;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

Results from another top level iteration.
Consolidates uu/top level vref netlist change to .0
picks up latest simulation wrappers and Makefile:

      euterepe_wrap.V
      i_s_euterpe_wrap.tb
      Makefile
----------------------------
revision 3.896
date: 1995/07/06 02:15:43;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V:
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
----------------------------
revision 3.895
date: 1995/07/05 18:32:32;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Release cerbrupttest
----------------------------
revision 3.894
date: 1995/07/04 22:44:36;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

consolidate latest top level route.  Includes hc bug fix
----------------------------
revision 3.893
```

```
date: 1995/07/03 23:03:08;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

chip_euterpe-base.* : manual cut-in of latest hc
Makefile.tst: backout latest change in net_xlimit
hc/hc0_control.pim: move uivalid1h to avoid toplevel collisions
----------------------------
revision 3.892
date: 1995/07/03 21:19:40;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests:
brconflictEasy.report:PASS
gauntlet-6-6-1.report:PASS
gauntlet-6-6-2.report:PASS
hexratio-100.report:PASS
stompratio.report:PASS
termite.report:PASS
----------------------------
revision 3.891
date: 1995/07/03 00:49:54;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

latest top level routing.  Pick up hc fix
----------------------------
revision 3.890
date: 1995/07/02 05:06:03;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/BOM,v
Working file: verify/BOM
head: 12.34
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 404;   selected revisions: 1
description:
```

```
----------------------------
revision 4.194
date: 1995/07/05 18:32:09;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Release cerbrupttest
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile.cmp,v
Working file: verify/Makefile.cmp
head: 4.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 1
description:
----------------------------
revision 4.4
date: 1995/07/05 22:32:00;  author: dit00;  state: Exp;  lines: +4 -4
Change to use likedriver commit
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/Makefile.defs,v
Working file: verify/Makefile.defs
head: 1.43
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 43;    selected revisions: 1
description:
----------------------------
revision 1.39
date: 1995/07/05 22:30:54;  author: dit00;  state: Exp;  lines: +3 -1
Add definitions for likedriver commit
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/config/Attic/i_h_euterpe_wrap.parm,v
Working file: verify/config/i_h_euterpe_wrap.parm
head: 5.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 5.1
date: 1995/07/04 05:07:19;  author: lisar;  state: Exp;
Added snoopy and hermes configurations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/config/i_s_euterpe_wrap.parm,v
Working file: verify/config/i_s_euterpe_wrap.parm
head: 5.2
branch:
```

```
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 5.1
date: 1995/07/04 05:07:21;  author: lisar;  state: Exp;
Added snoopy and hermes configurations.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/obj/processor/inst/Makefile,v
Working file: verify/obj/processor/inst/Makefile
head: 1.182
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 182;   selected revisions: 2
description:
----------------------------
revision 1.174
date: 1995/07/06 20:13:41;  author: jeffm;  state: Exp;  lines: +3 -3
Make doublemctest use the no-response offset in snoopy.
Add doublemctest2 - check handling two of the same type of problems,
sequentially.
Add triplemctest - ditto for three of the same type, sequentially.
----------------------------
revision 1.173
date: 1995/07/03 16:53:57;  author: dit00;  state: Exp;  lines: +2 -2
Added ltlbeasy.S, gltlbeasy.S to simple
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/random/template,v
Working file: verify/random/template
head: 2.33
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 33;    selected revisions: 1
description:
----------------------------
revision 2.15
date: 1995/07/05 22:54:55;  author: dit00;  state: Exp;  lines: +7 -7
Update template
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/BOM,v
Working file: verify/standalone/BOM
head: 6.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 85;    selected revisions: 1
description:
```

```
----------------------------
revision 4.34
date: 1995/07/05 18:31:55;  author: lisar;  state: Exp;  lines: +2 -2
Release Target: euterpe/verify/standalone/uu

Release cerbrupttest
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/BOM,v
Working file: verify/standalone/uu/BOM
head: 18.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 35;    selected revisions: 2
description:
releasebom adding BOM
----------------------------
revision 17.0
date: 1995/07/05 18:31:42;  author: lisar;  state: Exp;  lines: +1 -1
Release Target: euterpe/verify/standalone/uu

Release cerbrupttest
----------------------------
revision 16.1
date: 1995/07/05 18:31:34;  author: lisar;  state: Exp;  lines: +10 -10
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/standalone/uu/clean-request,v
Working file: verify/standalone/uu/clean-request
head: 6.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 6;     selected revisions: 1
description:
----------------------------
revision 6.6
date: 1995/07/05 18:30:38;  author: lisar;  state: Exp;  lines: +1 -0
clean build
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/cmpregcommit,v
Working file: verify/tools/cmpregcommit
head: 3.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 1
description:
----------------------------
revision 3.6
date: 1995/07/06 20:23:39;  author: doi;  state: Exp;  lines: +2 -0
```

```
make all register values lower case
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/likelevellog,v
Working file: verify/tools/likelevellog
head: 3.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 2
description:
----------------------------
revision 3.5
date: 1995/07/06 21:12:25;  author: doi;  state: Exp;  lines: +10 -8
ikos cylinder num is 1 off from zycad
----------------------------
revision 3.4
date: 1995/07/05 23:25:09;  author: doi;  state: Exp;  lines: +143 -82
handle both ikos and zycad inputs
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/tools/parselikedriver,v
Working file: verify/tools/parselikedriver
head: 8.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 2
description:
----------------------------
revision 8.3
date: 1995/07/06 22:48:48;  author: doi;  state: Exp;  lines: +1 -1
use the proper value for event mode
----------------------------
revision 8.2
date: 1995/07/06 01:04:03;  author: doi;  state: Exp;  lines: +8 -5
no longer try to support levellog utility. Also uses slightly faster method
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/Makefile,v
Working file: verify/toplevel/Makefile
head: 1.185
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 185;   selected revisions: 2
description:
----------------------------
revision 1.174
date: 1995/07/06 20:13:41;  author: jeffm;  state: Exp;  lines: +3 -3
Make doublemctest use the no-response offset in snoopy.
Add doublemctest2 - check handling two of the same type of problems,
sequentially.
Add triplemctest - ditto for three of the same type, sequentially.
```

```
----------------------------
revision 1.173
date: 1995/07/03 16:53:57;  author: dit00;  state: Exp;  lines: +2 -2
Added ltlbeasy.S, gltlbeasy.S to simple
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/cerbparerr.S,v
Working file: verify/toplevel/cerbparerr.S
head: 40.3
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 3;     selected revisions: 1
description:
----------------------------
revision 40.2
date: 1995/07/06 18:32:15;  author: jeffm;  state: Exp;  lines: +2 -2
Fix typo.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/doublemctest.S,v
Working file: verify/toplevel/doublemctest.S
head: 26.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 26.7
date: 1995/07/06 20:13:45;  author: jeffm;  state: Exp;  lines: +6 -3
Make doublemctest use the no-response offset in snoopy.
Add doublemctest2 - check handling two of the same type of problems,
sequentially.
Add triplemctest - ditto for three of the same type, sequentially.
----------------------------
revision 26.6
date: 1995/07/05 22:32:30;  author: lisar;  state: Exp;  lines: +2 -1
r32 was uninitialized
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/doublemctest2.S,v
Working file: verify/toplevel/doublemctest2.S
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/06 20:13:47;  author: jeffm;  state: Exp;
Make doublemctest use the no-response offset in snoopy.
```

```
Add doublemctest2 - check handling two of the same type of problems,
sequentially.
Add triplemctest - ditto for three of the same type, sequentially.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/template,v
Working file: verify/toplevel/template
head: 1.148
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 148;   selected revisions: 4
description:
----------------------------
revision 1.115
date: 1995/07/05 19:30:39;  author: dit00;  state: Exp;  lines: +102 -90
More hwterp status
----------------------------
revision 1.114
date: 1995/07/05 17:14:49;  author: lisar;  state: Exp;  lines: +65 -65
Updated to add some of the i_h and i_s groups
----------------------------
revision 1.113
date: 1995/07/03 22:45:42;  author: dit00;  state: Exp;  lines: +52 -52
hwterp status update
----------------------------
revision 1.112
date: 1995/07/03 16:33:45;  author: dit00;  state: Exp;  lines: +132 -132
update hwterp status, added hwfail and dne(does not exist)
=============================================================================

RCS file: /s6/cvsroot/euterpe/verify/toplevel/triplemctest.S,v
Working file: verify/toplevel/triplemctest.S
head: 41.1
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1;     selected revisions: 1
description:
----------------------------
revision 41.1
date: 1995/07/06 20:13:49;  author: jeffm;  state: Exp;
Make doublemctest use the no-response offset in snoopy.
Add doublemctest2 - check handling two of the same type of problems,
sequentially.
Add triplemctest - ditto for three of the same type, sequentially.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/BOM,v
Working file: verilog/BOM
head: 6.9
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 1390;  selected revisions: 8
description:
top level verilog BOM
----------------------------
revision 3.663
date: 1995/07/07 01:47:20;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at
      Makefile

at/Makefile:  Didn't have $(PERL) selecting the interpreter for
   at/genatpasel.pl, allowing it to select its own and depend on it
   being of executable file mode.
----------------------------
revision 3.662
date: 1995/07/06 06:05:10;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

Results from another top level iteration.
Consolidates uu/top level vref netlist change to .0
picks up latest simulation wrappers and Makefile:

      euterepe_wrap.V
      i_s_euterpe_wrap.tb
      Makefile
----------------------------
revision 3.661
date: 1995/07/06 02:15:17;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V:
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
----------------------------
revision 3.660
date: 1995/07/04 22:44:14;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

consolidate latest top level route.  Includes hc bug fix
----------------------------
revision 3.659
date: 1995/07/03 23:02:47;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

chip_euterpe-base.* : manual cut-in of latest hc
Makefile.tst: backout latest change in net_xlimit
hc/hc0_control.pim: move uivalid1h to avoid toplevel collisions
----------------------------
revision 3.658
date: 1995/07/03 21:19:20;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
```

```
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests:
brconflictEasy.report:PASS
gauntlet-6-6-1.report:PASS
gauntlet-6-6-2.report:PASS
hexratio-100.report:PASS
stompratio.report:PASS
termite.report:PASS
----------------------------
revision 3.657
date: 1995/07/03 00:49:32;  author: tbr;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc

latest top level routing.  Pick up hc fix
----------------------------
revision 3.656
date: 1995/07/02 05:05:42;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/BOM,v
Working file: verilog/bsrc/BOM
head: 346.6
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 1737;  selected revisions: 13
description:
----------------------------
revision 330.1
date: 1995/07/07 01:47:00;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at
      Makefile

at/Makefile:  Didn't have $(PERL) selecting the interpreter for
   at/genatpasel.pl, allowing it to select its own and depend on it
   being of executable file mode.
----------------------------
revision 330.0
date: 1995/07/06 06:04:47;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
Results from another top level iteration.
Consolidates uu/top level vref netlist change to .0
picks up latest simulation wrappers and Makefile:

      euterepe_wrap.V
      i_s_euterpe_wrap.tb
      Makefile
----------------------------
revision 329.1
date: 1995/07/06 06:04:30;  author: tbr;  state: Exp;  lines: +8 -8
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 329.0
date: 1995/07/06 02:14:52;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V:
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
----------------------------
revision 328.1
date: 1995/07/06 02:14:34;  author: mws;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 328.0
date: 1995/07/04 22:43:51;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

consolidate latest top level route.  Includes hc bug fix
----------------------------
revision 327.1
date: 1995/07/04 22:43:36;  author: tbr;  state: Exp;  lines: +15 -14
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 327.0
date: 1995/07/03 23:02:26;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

chip_euterpe-base.* : manual cut-in of latest hc
Makefile.tst: backout latest change in net_xlimit
hc/hc0_control.pim: move uivalid1h to avoid toplevel collisions
----------------------------
revision 326.2
date: 1995/07/03 23:02:10;  author: woody;  state: Exp;  lines: +6 -6
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 326.1
date: 1995/07/03 21:19:02;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
```

```
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests:
brconflictEasy.report:PASS
gauntlet-6-6-1.report:PASS
gauntlet-6-6-2.report:PASS
hexratio-100.report:PASS
stompratio.report:PASS
termite.report:PASS
----------------------------
revision 326.0
date: 1995/07/03 00:49:04;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

latest top level routing.  Pick up hc fix
----------------------------
revision 325.2
date: 1995/07/03 00:48:48;  author: tbr;  state: Exp;  lines: +12 -11
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 325.1
date: 1995/07/02 05:05:23;  author: woody;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/hc

hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile,v
Working file: verilog/bsrc/Makefile
head: 1.255
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 255;   selected revisions: 2
description:
----------------------------
revision 1.249
date: 1995/07/05 03:46:40;  author: lisar;  state: Exp;  lines: +10 -15
Don't use SCOUT as default
----------------------------
revision 1.248
date: 1995/07/04 01:13:30;  author: lisar;  state: Exp;  lines: +17 -5
Added i_s and i_h and targets. Added def SCOUT to i_ target
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.tst,v
```

```
Working file: verilog/bsrc/Makefile.tst
head: 40.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 7
description:
----------------------------
revision 40.94
date: 1995/07/05 03:12:34;  author: tbr;  state: Exp;  lines: +10 -93
clean up some obsolete junk
----------------------------
revision 40.93
date: 1995/07/04 22:12:11;  author: tbr;  state: Exp;  lines: +96 -89
comment out some obsolete stuff for testing.  Clean up shortly
----------------------------
revision 40.92
date: 1995/07/03 15:41:29;  author: tbr;  state: Exp;  lines: +8 -8
backout latest change in net_xlimit
----------------------------
revision 40.91
date: 1995/07/03 00:11:07;  author: tbr;  state: Exp;  lines: +8 -9
make splvsnetlist in parallel with route
----------------------------
revision 40.90
date: 1995/07/02 23:56:45;  author: tbr;  state: Exp;  lines: +8 -8
increase net_xlimit to 168
----------------------------
revision 40.89
date: 1995/07/02 19:01:22;  author: tbr;  state: Exp;  lines: +22 -6
patch up power.tab.top rule so it works for hc and io cases.
----------------------------
revision 40.88
date: 1995/07/01 21:32:31;  author: tbr;  state: Exp;  lines: +51 -28
 increase NET_XLIMIT to 150. order short.net file by slack
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Makefile.vo,v
Working file: verilog/bsrc/Makefile.vo
head: 27.45
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 45;    selected revisions: 2
description:
----------------------------
revision 27.42
date: 1995/07/05 03:12:32;  author: tbr;  state: Exp;  lines: +2 -3
clean up some obsolete junk
----------------------------
revision 27.41
date: 1995/07/04 11:25:30;  author: tbr;  state: Exp;  lines: +2 -2
correct problem when .pif.everything was unconditionally touched
=============================================================================
```

```
RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.netcap,v
Working file: verilog/bsrc/chip_euterpe-base.netcap
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 5
description:
----------------------------
revision 312.10
date: 1995/07/07 04:21:54;  author: tbr;  state: Exp;  lines: +40565 -40583
one more turn of the crank
----------------------------
revision 312.9
date: 1995/07/06 05:46:53;  author: tbr;  state: Exp;  lines: +47418 -47467
yet another iteration
----------------------------
revision 312.8
date: 1995/07/04 22:17:18;  author: tbr;  state: Exp;  lines: +3757 -3723
latest base files.  linsearch down to 1098 unroutes
----------------------------
revision 312.7
date: 1995/07/03 15:46:20;  author: tbr;  state: Exp;  lines: +4328 -4270
manual cut in of new hc
----------------------------
revision 312.6
date: 1995/07/03 00:03:07;  author: tbr;  state: Exp;  lines: +88214 -75405
from latest iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.nof,v
Working file: verilog/bsrc/chip_euterpe-base.nof
head: 307.11
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
----------------------------
revision 307.10
date: 1995/07/04 22:25:05;  author: tbr;  state: Exp;  lines: +40854 -40828
latest base files.  linsearch down to 1098 unroutes
----------------------------
revision 307.9
date: 1995/07/03 00:12:21;  author: tbr;  state: Exp;  lines: +33035 -33035
from latest iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.pim,v
Working file: verilog/bsrc/chip_euterpe-base.pim
head: 312.23
branch:
locks: strict
access list:
keyword substitution: kv
```

```
total revisions: 23;    selected revisions: 4
description:
----------------------------
revision 312.11
date: 1995/07/07 04:29:22;  author: tbr;  state: Exp;  lines: +1 -1
one more turn of the crank
----------------------------
revision 312.10
date: 1995/07/04 22:29:18;  author: tbr;  state: Exp;  lines: +362 -303
latest base files.  linsearch down to 1098 unroutes
----------------------------
revision 312.9
date: 1995/07/03 15:43:03;  author: tbr;  state: Exp;  lines: +251 -240
manual cut in of new hc
----------------------------
revision 312.8
date: 1995/07/03 00:16:43;  author: tbr;  state: Exp;  lines: +2 -2
from latest iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.strength,v
Working file: verilog/bsrc/chip_euterpe-base.strength
head: 312.20
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 20;    selected revisions: 5
description:
----------------------------
revision 312.10
date: 1995/07/07 04:27:44;  author: tbr;  state: Exp;  lines: +1128 -1128
one more turn of the crank
----------------------------
revision 312.9
date: 1995/07/06 05:52:37;  author: tbr;  state: Exp;  lines: +6872 -6881
yet another iteration
----------------------------
revision 312.8
date: 1995/07/04 22:31:20;  author: tbr;  state: Exp;  lines: +443 -424
latest base files.  linsearch down to 1098 unroutes
----------------------------
revision 312.7
date: 1995/07/03 15:53:20;  author: tbr;  state: Exp;  lines: +2930 -2930
manual cut in of new hc
----------------------------
revision 312.6
date: 1995/07/03 00:18:31;  author: tbr;  state: Exp;  lines: +58115 -50008
from latest iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/chip_euterpe-base.xrf,v
Working file: verilog/bsrc/chip_euterpe-base.xrf
head: 307.11
branch:
locks: strict
access list:
```

```
keyword substitution: kv
total revisions: 11;    selected revisions: 2
description:
----------------------------
revision 307.10
date: 1995/07/04 22:33:57;  author: tbr;  state: Exp;  lines: +25253 -25249
latest base files.  linsearch down to 1098 unroutes
----------------------------
revision 307.9
date: 1995/07/03 00:21:45;  author: tbr;  state: Exp;  lines: +25546 -25513
from latest iteration
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/e_mnemo_wrap.vhdl,v
Working file: verilog/bsrc/e_mnemo_wrap.vhdl
head: 308.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 308.2
date: 1995/07/07 05:59:26;  author: lisar;  state: Exp;  lines: +3 -2
Add poko
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe.V,v
Working file: verilog/bsrc/euterpe.V
head: 6.431
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 431;   selected revisions: 1
description:
----------------------------
revision 6.427
date: 1995/07/06 02:01:55;  author: mws;  state: Exp;  lines: +7 -2
uu/uu.V euterpe.V:
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/euterpe_wrap.V,v
Working file: verilog/bsrc/euterpe_wrap.V
head: 15.104
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 104;   selected revisions: 3
description:
```

```
----------------------------
revision 15.96
date: 1995/07/05 03:45:42;  author: lisar;  state: Exp;  lines: +6 -2
Oops forgot din1 on the interface
----------------------------
revision 15.95
date: 1995/07/04 01:08:49;  author: lisar;  state: Exp;  lines: +2 -2
Brought out to vhdl interface second hermes channel
----------------------------
revision 15.94
date: 1995/07/02 03:43:23;  author: lisar;  state: Exp;  lines: +26 -16
Add ifdef to hook scout_am to SC - run at ratio 3:1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/Attic/i_euterpe_mnemo_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_mnemo_wrap.tb
head: 308.2
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 2;     selected revisions: 1
description:
----------------------------
revision 308.2
date: 1995/07/07 06:01:17;  author: lisar;  state: Exp;  lines: +35 -11
Revisit hooking euterpe to mnemo - incorporate recent changes to other vhdl
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_euterpe_wrap.tb
head: 187.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 187.13
date: 1995/07/04 01:08:39;  author: lisar;  state: Exp;  lines: +6 -10
Brought out to vhdl interface second hermes channel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_euterpe_wrap.vhdl,v
Working file: verilog/bsrc/i_euterpe_wrap.vhdl
head: 187.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 1
description:
----------------------------
revision 187.13
date: 1995/07/04 01:08:42;  author: lisar;  state: Exp;  lines: +5 -1
Brought out to vhdl interface second hermes channel
```

```
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_h_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_h_euterpe_wrap.tb
head: 325.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 2
description:
----------------------------
revision 325.2
date: 1995/07/07 05:57:59;  author: lisar;  state: Exp;  lines: +31 -3
Add generics
----------------------------
revision 325.1
date: 1995/07/04 01:08:46;  author: lisar;  state: Exp;
Brought out to vhdl interface second hermes channel
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/i_s_euterpe_wrap.tb,v
Working file: verilog/bsrc/i_s_euterpe_wrap.tb
head: 325.5
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 5;     selected revisions: 3
description:
----------------------------
revision 325.3
date: 1995/07/05 19:21:25;  author: lisar;  state: Exp;  lines: +4 -2
Hook hermes channel 1 up with dummy5 and dummy6
----------------------------
revision 325.2
date: 1995/07/04 01:08:44;  author: lisar;  state: Exp;  lines: +6 -2
Brought out to vhdl interface second hermes channel
----------------------------
revision 325.1
date: 1995/07/01 17:42:03;  author: lisar;  state: Exp;
Add snoopy to the test bench
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/padtiles.ercf,v
Working file: verilog/bsrc/padtiles.ercf
head: 168.8
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 8;     selected revisions: 2
description:
----------------------------
revision 168.8
date: 1995/07/04 05:19:41;  author: tbr;  state: Exp;  lines: +3 -3
delete routorder.  Obsolete with netflag set to -1
```

```
----------------------------
revision 168.7
date: 1995/07/01 21:31:12;  author: tbr;  state: Exp;  lines: +18 -13
re-enable maze.  change maze netflag to -1
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/BOM,v
Working file: verilog/bsrc/at/BOM
head: 93.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 184;   selected revisions: 1
description:
releasebom adding BOM
----------------------------
revision 91.1
date: 1995/07/07 01:46:36;  author: mws;  state: Exp;  lines: +2 -2
Release Target: euterpe/verilog/bsrc/at
      Makefile

at/Makefile:  Didn't have $(PERL) selecting the interpreter for
   at/genatpasel.pl, allowing it to select its own and depend on it
   being of executable file mode.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/at/Makefile,v
Working file: verilog/bsrc/at/Makefile
head: 1.18
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 18;    selected revisions: 1
description:
----------------------------
revision 1.18
date: 1995/07/07 01:45:47;  author: mws;  state: Exp;  lines: +2 -2
Didn't have $(PERL) selecting the interpreter for at/genatpasel.pl, allowing
it to select its own and depend on it being of executable file mode.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/BOM,v
Working file: verilog/bsrc/hc/BOM
head: 125.0
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 250;   selected revisions: 8
description:
releasebom adding BOM
----------------------------
revision 121.0
date: 1995/07/03 22:58:47;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc
```

```
chip_euterpe-base.* : manual cut-in of latest hc
Makefile.tst: backout latest change in net_xlimit
hc/hc0_control.pim: move uivalid1h to avoid toplevel collisions
----------------------------
revision 120.1
date: 1995/07/03 22:58:38;  author: woody;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 120.0
date: 1995/07/03 21:18:43;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests:
brconflictEasy.report:PASS
gauntlet-6-6-1.report:PASS
gauntlet-6-6-2.report:PASS
hexratio-100.report:PASS
stompratio.report:PASS
termite.report:PASS
----------------------------
revision 119.1
date: 1995/07/03 21:18:34;  author: woody;  state: Exp;  lines: +5 -5
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 119.0
date: 1995/07/03 00:29:25;  author: tbr;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

latest top level routing.  Pick up hc fix
----------------------------
revision 118.1
date: 1995/07/03 00:29:16;  author: tbr;  state: Exp;  lines: +3 -3
releasebom: File needs to be up-to-date to use commit -r
----------------------------
revision 118.0
date: 1995/07/02 05:05:03;  author: woody;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc/hc

hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
----------------------------
```

```
revision 117.1
date: 1995/07/02 05:04:56;  author: woody;  state: Exp;  lines: +4 -4
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc.V,v
Working file: verilog/bsrc/hc/hc.V
head: 1.56
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 56;    selected revisions: 1
description:
----------------------------
revision 1.56
date: 1995/07/03 21:14:32;  author: woody;  state: Exp;  lines: +14 -9
hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0.power.tab.top,v
Working file: verilog/bsrc/hc/hc0.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 68.9
date: 1995/07/02 18:59:48;  author: tbr;  state: Exp;  lines: +272 -942
update from latest top level
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc0_control.pim,v
Working file: verilog/bsrc/hc/hc0_control.pim
head: 73.25
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 25;    selected revisions: 3
description:
----------------------------
revision 73.25
date: 1995/07/03 22:40:32;  author: woody;  state: Exp;  lines: +1 -1
move uivalid1h to avoid toplevel collisions.
```

```
----------------------------
revision 73.24
date: 1995/07/03 21:14:36;  author: woody;  state: Exp;  lines: +12 -3
hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests.
----------------------------
revision 73.23
date: 1995/07/02 04:36:22;  author: woody;  state: Exp;  lines: +4 -4
hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1.power.tab.top,v
Working file: verilog/bsrc/hc/hc1.power.tab.top
head: 68.9
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 9;     selected revisions: 1
description:
----------------------------
revision 68.9
date: 1995/07/02 18:59:58;  author: tbr;  state: Exp;  lines: +322 -3263
update from latest top level
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc1_control.pim,v
Working file: verilog/bsrc/hc/hc1_control.pim
head: 73.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 2
description:
----------------------------
revision 73.15
date: 1995/07/03 21:14:39;  author: woody;  state: Exp;  lines: +11 -2
hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
```

```
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests.
----------------------------
revision 73.14
date: 1995/07/02 04:36:26;  author: woody;  state: Exp;  lines: +4 -4
hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/hc/hc_parse.Veqn,v
Working file: verilog/bsrc/hc/hc_parse.Veqn
head: 3.15
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 15;    selected revisions: 2
description:
----------------------------
revision 3.15
date: 1995/07/03 21:14:43;  author: woody;  state: Exp;  lines: +5 -5
hc.V,hc_parse.Veqn: worst case prb grant to timing can result in lost data when
back-to-back responses are being received from the channel. In the worst case
the prbd{01}1 register will be overwritten before the second half of the data
is selected onto the prb. Added idata9 and delayed the control by 1 cycle. The
addition of idata9 also caused the addition of another copy of ivalid to
prevent a dc load violation.

Placement updated.

passed multiple standalone tests.
----------------------------
revision 3.14
date: 1995/07/02 04:36:28;  author: woody;  state: Exp;  lines: +12 -15
hc_parse.Veqn: stompprb signal not available soon enough to 'stomp' an
immediate prb grant, thus prb response sent to nb twice. standalone test
gauntlet (with option START_PHASE=2) detected. Since stompprb couldn't be avail
1 cyle eariler (pla explosion), rxend had to be asserted 1-cycle later to
prevent prbctrl from sending packet. This has a minor negative impact on
performance (more wasted prb bandwidth).

Placement updated, 4 cells removed from both pim files.
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/BOM,v
Working file: verilog/bsrc/uu/BOM
head: 218.1
```

```
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 480;   selected revisions: 2
description:
----------------------------
revision 213.0
date: 1995/07/06 02:12:52;  author: mws;  state: Exp;  lines: +1 -1
Release Target: euterpe/verilog/bsrc

uu/uu.V euterpe.V:
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
----------------------------
revision 212.1
date: 1995/07/06 02:12:39;  author: mws;  state: Exp;  lines: +2 -2
releasebom: File needs to be up-to-date to use commit -r
=============================================================================

RCS file: /s6/cvsroot/euterpe/verilog/bsrc/uu/uu.V,v
Working file: verilog/bsrc/uu/uu.V
head: 1.202
branch:
locks: strict
access list:
keyword substitution: kv
total revisions: 202;   selected revisions: 1
description:
issue unit
----------------------------
revision 1.199
date: 1995/07/06 02:02:34;  author: mws;  state: Exp;  lines: +9 -4
   Explicitly bring vref_0ph into uu because it needs some concatenations
   including VRef, but verilog won't let us leave nulls (the usual
   convention to get emerge/topt to tie a floating pin to VRef) in a
   concatenation, and topt/emerge won't recognize/flatten a nonnull VRef
   netname except at top level.  Should fix "float input" csyn error.
=============================================================================
```